REMARKS

Prior to the present amendment, claims 1-7, 9, 11, 13, and 20-23 were pending in the present application. By this amendment, Applicant has amended claim 1. Thus, claims 1-7, 9, 11, 13, and 20-23 remain in the present application. Reconsideration and allowance of pending claims 1-7, 9, 11, 13, and 20-23 in view of the above amendments and the following remarks are requested.

A. Rejection of Claims 1-7, 9, 11, 13, and 20-23 under 35 USC §103(a)

The Examiner has rejected claims 1-7, 9, 11, 13, and 20-23 under 35 USC §103(a) as being unpatentable over U.S. patent number 6,740,952 B2 to Fujishima et al. (hereinafter "Fujishima") in view of U.S. patent number 6,525,390 B2 to Tada et al. (hereinafter "Tada"), U.S. patent number 6,639,277 B2 to Rumennik et al. (hereinafter "Rumennik"), *Microchip Fabrication: A Practical Guide to Semiconductor Processing*, 2000, Mc-Graw Hill, New York, 4th Edition, pp. 382,511, by Peter Van Zant (hereinafter "Zant"), *VLSI Fabrication Principles: Silicon and Gallium Arsenide*, 1994, John Wiley & Sons, Inc., New York, 2nd Edition, pp. 258-259, by Sorab K. Ghandhi (hereinafter "Ghandhi"), U.S. patent number 6,617,652 B2 to Masaaki Noda (hereinafter "Noda"), and U.S. patent number 5,801,431 to Niraj Ranjan (hereinafter "Ranjan"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claim 1, is patentably distinguishable over Fujishima,

Tada, Rumennik, Zant, Ghandhi, Noda, and Ranjan, either singly or in any combination thereof.

The present invention, as defined by amended independent claim 1, provides a resurf region formed over at least a portion of a drift region in an epitaxially formed semiconductor layer between a body region and a drain region, and a field plate structure disposed over the resurf region, where the field plate structure includes a first field plate including a first portion spaced from a second portion by a first gap, a second field plate including a first portion spaced from a second portion by a second gap, and a third field plate including a first portion spaced from a second portion by a third gap, and where the second portion of the first field plate is electrically connected to the drain region. As disclosed in the present application, in an embodiment of the invention, a field plate structure is formed over resurf region 30, where the field plate structure includes a first field plate having first portion 32 and second portion 33 spaced from its first portion 32 by gap 39, a second field plate having first portion 36 and second portion 38 spaced from its first portion 36 by gap 40, and a third field plate having first portion 42 and second portion 44 which is spaced for first portion 42 by gap 46. See, e.g., Figure 1 and related text of the present application.

As disclosed in the present application, the first field plate structure is disposed over resurf region 30, which is formed in epitaxially formed semiconductor layer 12 between drain region 26 and body region 14 over at least a portion of drift region 28, where second portion 33 of the first field plate is electrically connected to drain region 26

by electrical connectors 50 and second portion 38 of the second field plate structure. *See*, e.g., Figure 1 and related text of the present application. As disclosed in the present application, a field plate according to the present invention reduces the surface charge on the field insulation beneath each plate to advantageously permit the devices to withstand 650 V or more when applied in, for example, 0.35 micron CMOS. *See*, e.g., paragraph [0012] of the present application.

In contrast to the present invention as defined by amended independent claim 1, Fujishima does not disclose a resurf region formed over at least a portion of a drift region in an epitaxially formed semiconductor layer between a body region and a drain region, and a field plate structure disposed over the resurf region, where the field plate structure includes a first field plate including a first portion spaced from a second portion by a first gap, a second field plate including a first portion spaced from a second portion by a second gap, and a third field plate including a first portion spaced from a second portion by a third gap, and where the second portion of the first field plate is electrically connected to the drain region. Fujishima specifically discloses a semiconductor device including field plate FP1 disposed over interlayer insulating film 10 and electrically connected to gate electrode layer 9, field plate FP2 overlying field plate FP1 and electrically connected to source region 3, and field plate FP3 separated from second field plate FP2 by interval Wg, where field plate FP3 is electrically connected to drain region 6 by drain electrode layer 12. *See*, e.g., Figure 19 and related text of Fujishima.

In the outstanding Final Rejection, the Examiner argues that Fujishima discloses a field plate structure including "a first plate 9 disposed over the first insulation layer 8," "a second plate FP1 disposed over the second insulation layer 8," and "a third plate FP2/FP3 spaced from the second plate FP1 by the third insulation layer 24." *See* page 3 of the Final Rejection dated April 2, 2009. However, even if gate electrode 9 is considered a first plate as suggested by the Examiner, Fujishima fails to disclose a first plate having a second portion electrically connected to a drain region, as specified in amended independent claim 1. Fujishima also fails to disclose a resurf region formed over at least a portion of a drift region in an epitaxially formed semiconductor layer between a body region and a drain region, as specified in amended independent claim 1.

To overcome the acknowledged lack of a resurf region, the Examiner suggests combining Tada with Fujishima. Tada specifically discloses counter-doped region 44, which is formed by counter-doping p-type impurities to the surface portion of n-type offset region 3 formed in substrate 1. *See*, e.g., Figures 9 and 10 and related text of Tada. In Tada, counter-doped region 44 has a p-type impurity concentration of $3x10^{16}$ cm^{-3}. *See*, e.g., column 12, lines 17-28 of Tada. However, as disclosed in Ranjan (cited by the Examiner), high breakdown voltage is achieved when the charge in the top resurf layer is controlled at approximately $1x10^{12}$ cm^2 and the charge in the lower resurf region is controlled at 1.5 to $2x10^{12}$ cm^2. *See*, e.g., column 1, lines 33-37 of Ranjan. Thus, Applicant submits that counter-doped region 44 is not a resurf region, as specified in

amended independent claim 1. Thus, neither Tada nor Fujishima disclose a resurf region over a drift region, as specified in amended independent claim 1.

To overcome the acknowledged lack of a first plate including a second portion spaced from the first portion of the first plate by a first gap, the Examiner suggests combining Rumennik with Fujishima. Rumennik specifically discloses gate 12 and field plate member 26 situated over thick oxide layer 40, where field plate member 26 is spaced apart from gate 12, and where field plate member 26 is electrically connected to drain electrode 11. However, the structure disclosed in Rumennik is significantly different than the structure disclosed in Fujishima. In particular, in Fujishima, gate electrode 9 is electrically connected to field plate FP1, whereas gate 12 is not connected to a field plate. Also, in Fujishima, field plate FP2 overlies filed plate FP1 and is electrically connected to source region 3. In contrast, source electrode 10 and drain electrode 11 in Rumennik are separated by a space over dielectric layer 27. Thus, Applicant submits that a person of ordinary skill in the art, at the time the invention defined by amended independent claim 1 was made, would not reasonably combine Rumennik with Fujishima as suggested by the Examiner.

Also none of Zant, Ghandhi, Noda, and Ranjan discloses a resurf region formed over at least a portion of a drift region in an epitaxially formed semiconductor layer between a body region and a drain region, and a field plate structure disposed over the resurf region, where the field plate structure includes a first field plate including a first portion spaced from a second portion by a first gap, a second field plate including a first

portion spaced from a second portion by a second gap, and a third field plate including a first portion spaced from a second portion by a third gap, and where the second portion of the first field plate is electrically connected to the drain region, as specified in amended independent claim 1. Thus, Applicant submits that the combination of Fujishima, Tada, Rumennik, Zant, Ghandhi, Noda, and Ranjan fail to make obvious the present invention as defined by amended independent claim 1.

Additionally, Applicant submits that a person of ordinary skill in the art, at the time the invention defined by amended independent claim 1 was made, would not reasonably combine Fujishima, Tada, Rumennik, Zant, Ghandhi, Noda, and Ranjan, as suggested by the Examiner. Thus, Applicant submits that the teachings suggested by the Examiner (i.e. the combination of Fujishima, Tada, Rumennik, Zant, Ghandhi, Noda, and Ranjan) are based on a classic hindsight reconstruction given the benefit of Applicant's disclosure, which is impermissible.

For all the foregoing reasons, Applicant respectfully submits that, at the time the invention defined by amended independent claim 1 was made, the invention would not have been obvious to a person of ordinary skill in the art by Fujishima, Tada, Rumennik, Zant, Ghandhi, Noda, and Ranjan, either singly or in any combination thereof. Thus, amended independent claim 1 is patentably distinguishable over Fujishima, Tada, Rumennik, Zant, Ghandhi, Noda, and Ranjan and, as such, claims 2-7, 9, 11, 13, and 20-23 depending from amended independent claim 1 are, *a fortiori*, also patentably distinguishable over Fujishima, Tada, Rumennik, Zant, Ghandhi, Noda, and Ranjan for at

least the reasons presented above and also for additional limitations contained in each dependent claim.

B. Conclusion

For all the foregoing reasons pending 1-7, 9, 11, 13, and 20-23 are patentably distinguishable over the cited art, and an early allowance of pending claims 1-7, 9, 11, 13, and 20-23 is respectfully requested.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

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Respectfully Submitted,
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